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THE UNITED STATES PATENT AND TRADEMARK OFFICE

REVOCATION AND NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

I, ***Dr. Graham Fisher, Director of Intellectual Property*** of ***MEMC Electronic Materials, Inc.***, the Assignee of the entire right, title, and interest in the ***U.S. Patent Application(s) and/or Patent(s) identified on the attached Schedule A***, hereby revoke all previous powers of attorney or authorizations of agent given and do hereby appoint the attorneys or agents associated with the following Customer Number, with full power of substitution and revocation, to prosecute and transact all business in the Patent and Trademark Office connected therewith for the ***U.S. Patent Application(s) and/or Patent(s) listed in the attached Schedule A:***

Customer Number: 76681

Please direct all correspondence in connection with said ***U.S. Patent Application(s) and/or Patent(s)*** to:

Customer Number: 76681

Respectfully submitted,

Date: 5/13/2008

Dr. Graham Fisher
Director of Intellectual Property
MEMC Electronic Materials, Inc.

PATENT

THE UNITED STATES PATENT AND TRADEMARK OFFICE

STATEMENT UNDER 37 CFR 3.73(b)

MEMC Electronic Materials, Inc., a Delaware Corporation, pursuant to 37 CFR 3.73(b), hereby states that it is the Assignee of the entire right, title, and interest in ***U.S. Patent Application(s) and/or Patent(s) on the attached Schedule A.***

The entire rights, title, and interest in the aforementioned Patent Application(s) and/or Patent(s) were conveyed to ***MEMC Electronic Materials, Inc.*** via Assignment(s) recorded with the United States Patent and Trademark Office at the ***Reel/Frame Numbers on the attached Schedule A.***

The undersigned, ***Dr. Graham Fisher, Director of Intellectual Property,*** has full authorization to act on behalf of Assignee ***MEMC Electronic Materials, Inc.***

Respectfully submitted,

Date: 5/13/2008

Dr. Graham Fisher
Director of Intellectual Property
MEMC Electronic Materials, Inc.

APPENDIX A
Owned by MEMC Electronic Materials, Inc.

ATTORNEY REFERENCE	CONF. NO	PUBLICATION NO. & DATE	SERIAL NO. FILING DATE	PATENT NO. ISSUE DATE	CURRENT OWNER/ ASSIGNEE	REEL AND FRAME NO.	TITLE
MEMC2495.1	9140	US-2002-0000185-A1 1/3/2002	09/929,585 8/14/2001	6,432,197 8/13/2002	MEMC Electronic Materials, Inc.	Continuation of 09/379,383 recorded at 010296/0838	PROCESS FOR THE PREPARATION OF NON-OXYGEN PRECIPITATING CZOCHRALSKI SILICON WAFERS
MEMC2495.2	1234	US-2002-0189528-A1 12/19/2002	10/217,703 8/13/2002	6,709,511 3/23/2004	MEMC Electronic Materials, Inc.	Continuation of 09/929,585 recorded at 010296/0838	PROCESS FOR SUPPRESSING OXYGEN PRECIPITATION IN VACANCY DOMINATED SILICON
MEMC2499	8355		09/404,428 9/23/1999	6,214,704 4/10/2001	MEMC Electronic Materials, Inc.	010379/0160	METHOD OF PROCESSING SEMICONDUCTOR WAFERS TO BUILD IN BACK SURFACE DAMAGE
MEMC2503	8725		09/385,108 8/27/1999	6,361,619 3/26/2002	MEMC Electronic Materials, Inc.	010330/0004	THERMALLY ANNEALED WAFERS HAVING IMPROVED INTERNAL GETTERING
MEMC2503.1	6207	US-2002-0170631-A1 11/21/2002	10/067,070 2/4/2002	6,686,260 2/3/2004	MEMC Electronic Materials, Inc.	Division of 09/385,108 recorded at 010330/0004	PROCESS FOR PRODUCING THERMALLY ANNEALED WAFERS HAVING IMPROVED INTERNAL GETTERING
MEMC2507	8140		09/384,669 8/27/1999	6,191,010 2/20/2001	MEMC Electronic Materials, Inc.	010724/0525	PROCESS FOR PREPARING AN IDEAL OXYGEN PRECIPITATING SILICON WAFER
MEMC2512	2402		09/387,288 8/31/1999	6,236,104 5/22/2001	MEMC Electronic Materials, Inc.	010449/0840	SILICON ON INSULATOR STRUCTURE FROM LOW DEFECT DENSITY SINGLE CRYSTAL SILICON
MEMC2512.1	9249	US-2001-0030348-A1 10/18/2001	09/737,715 12/15/2000	6,342,725 1/29/2002	MEMC Electronic Materials, Inc.	Continuation of 09/387,288 recorded at 010449/0840	SILICON ON INSULATOR STRUCTURE HAVING A LOW DEFECT DENSITY HANDLE WAFER AND PROCESS FOR THE PREPARATION THEREOF
MEMC2512.2	7363	US-2002-0113265-A1 8/22/2002	10/038,084 1/3/2002	6,849,901 2/1/2005	MEMC Electronic Materials, Inc.	Division of 09/737,715 which is a continuation of 09/387,288 recorded at 010449/0840	A SILICON-ON-INSULATOR STRUCTURE HAVING A DEVICE LAYER WHICH IS VACANCY DOMINATED AND SUBSTANTIALLY FREE OF AGGLOMERATED VACANCY-TYPE DEFECTS
MEMC2516	1795		09/432,928 11/3/1999	6,293,139 9/25/2001	MEMC Electronic Materials, Inc.	010459/0198	METHOD OF DETERMINING PERFORMANCE CHARACTERISTICS OF POLISHING PADS
MEMC2524	2877		09/507,811 2/22/2000	6,514,423 2/4/2003	MEMC Electronic Materials, Inc.	010627/0292	METHOD FOR WAFER PROCESSING
MEMC2553	7647		09/417,610 10/13/1999	6,284,039 9/4/2001	MEMC Electronic Materials, Inc.	010464/0549	EPITAXIAL SILICON WAFERS SUBSTANTIALLY FREE OF GROWN-IN DEFECTS
MEMC2553.1	6168	US-2001-0039916-A1 11/15/2001	09/874,487 6/5/2001	6,565,649 5/20/2003	MEMC Electronic Materials, Inc.	Continuation of 09/417,610 recorded at 010464/0549	AN EPITAXIAL WAFER SUBSTANTIALLY FREE OF GROWN-IN DEFECTS
MEMC2553.2	3406	US-2003-0205191-A1 11/6/2003	10/441,413 5/20/2003	7,097,718 8/29/2006	MEMC Electronic Materials, Inc.	Continuation of 09/874,487 which is a continuation of 09/417,610 recorded	SINGLE CRYSTAL SILICON WAFER HAVING AN EPITAXIAL LAYER SUBSTANTIALLY FREE FROM GROWN-IN DEFECTS